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System Framework for a Multi-Band, Multi-Mode Software Defined Radio

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14. ABSTRACT

This paper describes a system framework for a multi-band, multi-mode software defined radio (MBMM SDR) being developed for next-generation telemetry applications. The system framework consists of a multi-band front-end (MBFE), a multi-mode digital radio (MMDR), and configuration and control (C2) sub-systems. The MBFE consists of an L/S/C-band transceiver architecture that provides wideband operation, band selection, and channel tuning. The MMDR consists of the software and firmware components for high-speed digital signal processing for the telemetry waveforms. Finally, the C2 consists of the software and hardware components for system configuration, control and status. The MBFE is implemented as a stand-alone hardware sub-system, while the MMDR and C2 are integrated into a single hardware sub-system utilized state-of-the-art system-on-a-chip (SoC) technology. Design methodologies, hardware architectures, and system tradeoffs are highlighted to meet next-generation telemetry requirements for improved spectrum efficiency and utilizations.

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Spectrum, Aeronautical telemetry, algorithm, bandwidth, Integrated Networked Enhanced Telemetry (iNET), Shaped Offset Quadrature Phase Shift Keying (SOQPSK), bit error rate (BER), multi-band, multi-mode software defined radio (MBMM SDR), tri-band (L,S,C)

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SYSTEM FRAMEWORK FOR A MULTI-BAND, MULTI-MODE SOFTWARE DEFINED RADIO

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ABSTRACT

This paper describes a system framework for a multi-band, multi-mode software defined radio (MBMM SDR) being developed for next-generation telemetry applications. The system framework consists of a multi-band front-end (MBFE), a multi-mode digital radio (MMDR), and configuration and control (C2) sub-systems. The MBFE consists of an L/S/C-band transceiver architecture that provides wideband operation, band selection, and channel tuning. The MMDR consists of the software and firmware components for high-speed digital signal processing for the telemetry waveforms. Finally, the C2 consists of the software and hardware components for system configuration, control and status. The MBFE is implemented as a stand-alone hardware sub-system, while the MMDR and C2 are integrated into a single hardware sub-system utilized state-of-the-art system-on-a-chip (SoC) technology. Design methodologies, hardware architectures, and system tradeoffs are highlighted to meet next-generation telemetry requirements for improved spectrum efficiency and utilizations.

KEY WORDS

Multi-band Transceiver, Software-Defined Radio, C-Band Telemetry, System-on-a-Chip

INTRODUCTION

It is envision that next-generation telemetry infrastructure will be a net-centric architecture that optimizes spectrum efficiency and utilization due to the decreasing spectrum allocations for Department of Defense's (DoD) systems. To improve spectrum efficiency and utilization, the telemetry infrastructure must provide operational flexibility in frequency and modulation. As a result, Test Resource Management Center (TRMC) is supporting the development of a multi-band, multi-mode software defined radio (MBMM SDR) to demonstrate the next-generation radio segment for the net-centric telemetry infrastructure. The MBMM SDR operates across the L/S/C-Band telemetry allocations and provides advanced state-of-the-art system-on-a-chip (SoC) technology for multi-mode operations.

The system framework for the MBMM SDR is illustrated in Figure 1. The framework consists of three primary sub-systems: the multi-band front end (MBFE), the multi-mode digital radio (MMDR), and the configuration and control (C2). The MBFE provides wideband operation, band selection, and channel tuning that support L/S/C-band telemetry allocations. The MMDR implements field-programmable gate array (FPGA) technology to provide high-speed signal processing of Pulse Code Modulation/Frequency Modulation (PCM/FM) and Shaped Offset Quadrature Shift Keying (SOQPSK-TG) waveforms, respectively. The C2 consist of software and hardware for booting, configuration, control & status of MBFE and MMDR, and memory & filesystem management.

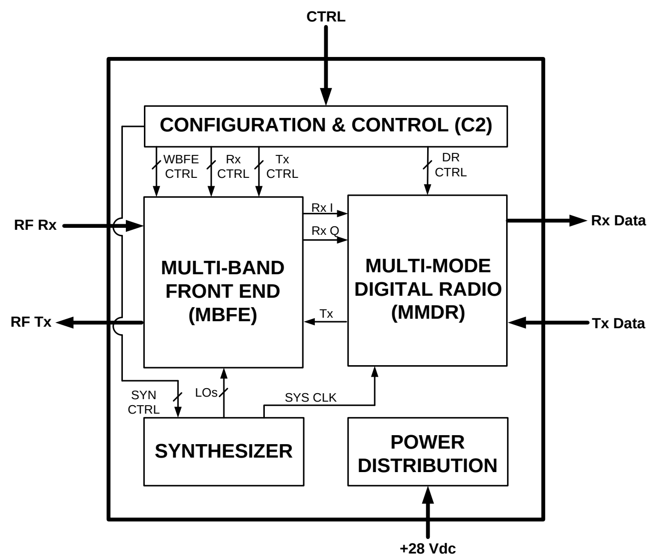

Figure 1: MBMM SDR System Framework

This paper highlights the design methodologies, hardware architectures, and system tradeoffs for each of primary sub-systems for the MBMM SDR. The MBFE is implemented as a stand-alone hardware sub-system consists of design tradeoff between two receiver (Rx) channel architectures and single transmitter (Tx) channel architecture. The MMDR and C2 are implemented into a single hardware sub-system consisting of two operation planes: the digital radio (DR) plane that hosts the telemetry waveform firmware, and the C2 plane that hosts the embedded software for the system configuration, control and status.

MULTI-BAND FRONT END

For this work, we are investigating two receiver (Rx) design methodologies to provide band selection and channel tuning within the telemetry allocations. The first design methodology is based on the Weaver architecture that utilizes image-rejection to provide band selection between L/S-Band and C-Band allocations, respectively. Detail explanations of the Weaver architecture and the design methodology are given in [1, 2]. The primary design objective is to develop a frequency plan that allows for the proper sideband relationship between the L/S-Band as the lower sideband (LSB) component and the C-Band as the upper sideband (USB) component to perform coarse selection using image-rejection. A simplified block diagram of the Weaver architecture is illustrated in Figure 2.

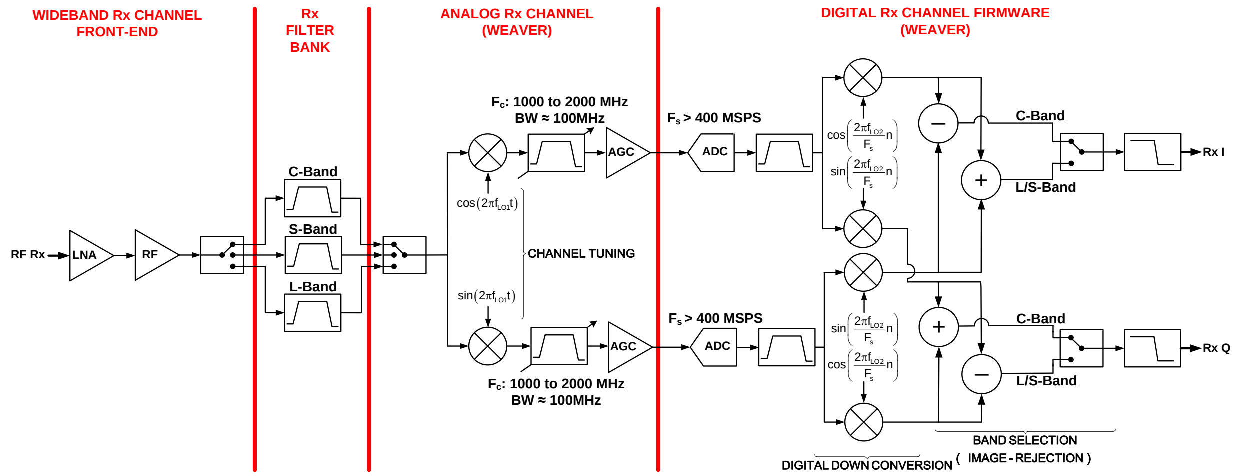

Figure 2: Weaver Rx Architecture

The hardware architecture consists of a wideband front-end, static filter bank, and the Weaver channel architecture. The wideband front-end is designed to provide continuous signal conditioning across the 1000 MHz to 6000 MHz spectrum, the static filter bank provides band selection based on the overall frequency allocation for each band. The Weaver channel architecture is a hybrid implementation between analog and digital components. The analog portion provides the initial frequency translation to the intermediate frequency (IF) that ensures proper sideband relationship for image-rejection [2]. The required IFs range from 1000 MHz to 2000 MHz based on the frequency separation of the L/S-band allocations and C-Band allocation. To accommodate this frequency range, adaptive band-pass filters (ABPF) components are implemented after the translation stage. After signal conditioning and data conversion, a secondary digital frequency translation and coarse sideband selection are performed based on [2]. The channelizer within the digital receiver performs channel selection within the 100-MHz channel bandwith.

The second Rx design methodology is based on an adaptive filter bank (AFB) architecture that utilizes the ABPF components. The ABPF is able to tune the center frequency and bandwidth to provide better selectivity based on the configuration mode (i.e. data rate, channel, and modulation). An analog frequency translation stage down converts the RF spectrum to a 100-MHz IF spectrum, which is filtered with a highly selective band-pass filter (BPF) centered at fixed 600 MHz as illustrated in Figure 3. A high-IF was selected to relax filtering requirements for local oscillator (LO) and image suppression. During data conversion, undersampling is utilized to centered the 100-MHz IF spectrum within the first Nyquist zone. As a result, a second-stage digital frequency translation is required to move the spectrum to baseband and provide I & Q paths for demodulation and detection within the digital receiver. As previously, the channelizer within the digital receiver performs channel selection within the 100-MHz channel bandwidth.

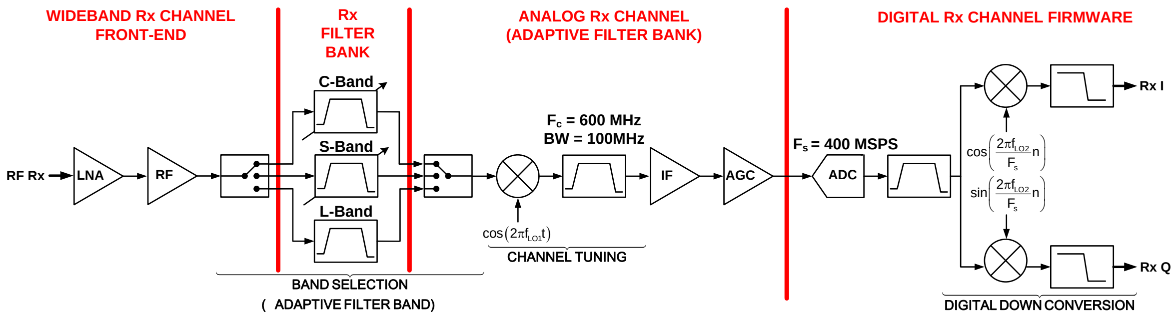

Figure 3: AFB Rx Architecture

The transmitter (Tx) design methodology is based on a high-IF architecture that relaxes the analog filtering requirements of the adaptive filter bank. The high-IF is achieved by selecting a high-order alias from the data conversion. To compensate for the digital-to-analog converter (DAC) roll-off effect, the DAC rate is selected to center the aliases within the centered of the Nyquist zones as illustrated in Figure 4. In addition, an inverse sinc compensate filter is implemented within the digital interpolation stage. An 600-MHz IF was selected based on a 400MHz DAC rate and 40 dB of attenuation by ABPFs at the LO frequencies. Channel selection within the 100-MHz channel bandwidth is performed by frequency offsetting to the digital baseband signal and analog frequency translating to the appropriate telemetry allocation.

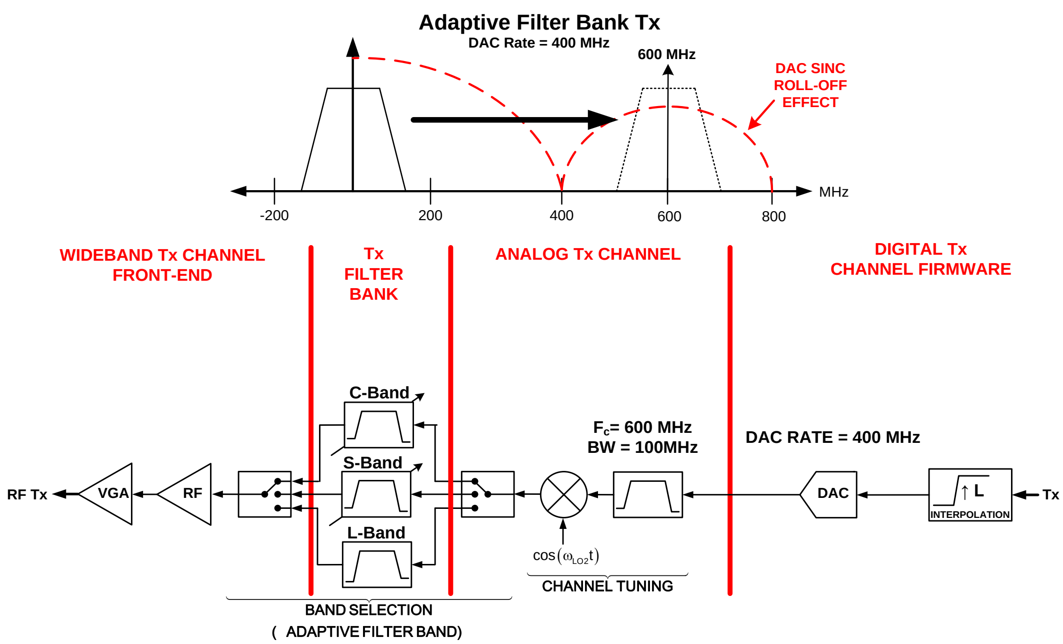

Figure 4: Tx Architecture

Circuit performance and analysis for the MBFE sub-systems are presented in [3]. In addition, optimization of the MBFE sub-systems is on-going for test range demonstration of the MMBM SDR using a C-12 aircraft in FY2015.

MULTI-MODE DIGITAL RADIO

The telemetry waveforms implemented are PCM/FM and SOQPSK-TG. Both waveforms are continuous phase modulation (CPM) that allows for common functionalities to be designed for both waveforms. The primary difference is the modulation technique: frequency vs. phase. However, frequency modulation can be implemented as a phase modulation since frequency is related to the change of phase. As a result, a common Tx path can be designed as illustrated in Figure 5. For SOQPSK, the differential encoder, Q-bit delay, and precoder are required per IRIG 106 specifications. In addition, the shaping filter is different for the telemetry waveforms: a 2-symbol length raised cosine (2RC) filter for PCM/FM and an 8-symbol length temporal raised cosine for SOQPSK. Detail specifications of the telemetry waveforms are given in [4].

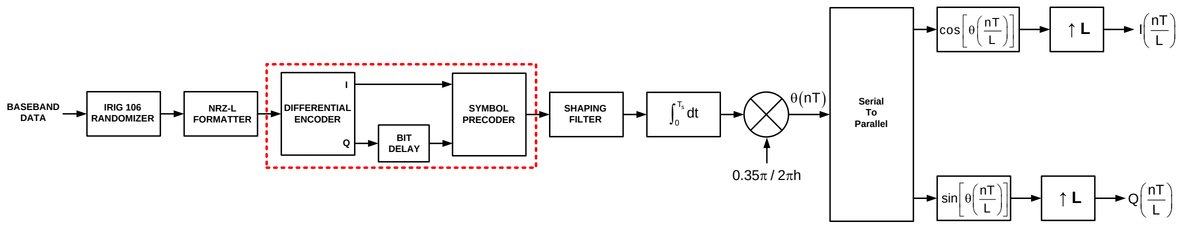

Figure 5: Tx-Path Common Hardware Architecture

The primary Rx functionalities include channelization, demodulation, and detection. Channelization selects the appropriate channel within the 100-MHz baseband spectrum from the MBFE. The channelizer was implemented using a filter bank architecture that translates the prototype filter to channel offset frequency. The occupied channel spectrum is based primary on the data rate and modulation configuration, which defined the filter requirements for the prototype filter. Once the channel is filtered, baseband translation is performed for demodulation and detection. Figure 6 & Figure 7 illustrates the design methodology and hardware architecture for the channelizer.

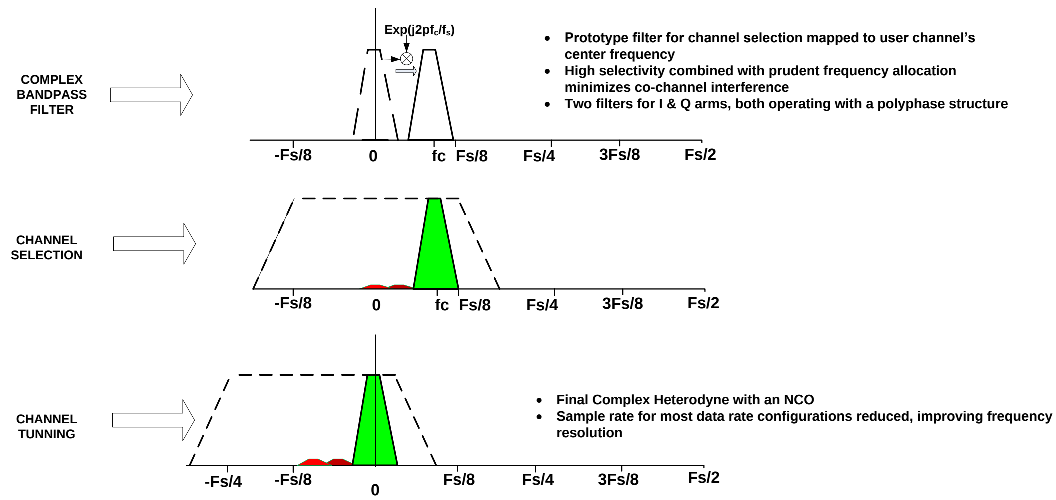

Figure 6: Channelizer Design Methodology

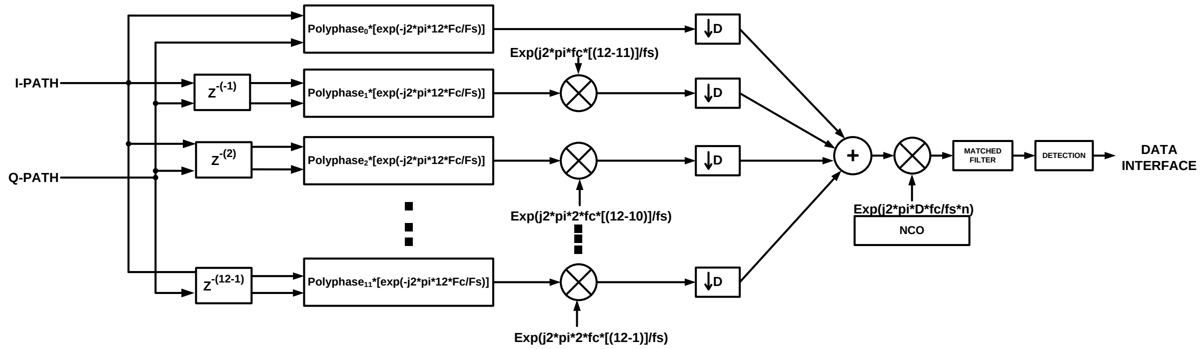

Figure 7: Channelizer Hardware Architecture

Demodulation and detection is based on match filter architecture with multi-symbol detection. First, carrier and phase synchronization is performed based on the phase statistics of the trellis decoder [5-7]. As a result, the numerically controlled oscillators (NCOs) are adjusted for demodulation of the baseband channel waveform. For optimum detector for CPM waveforms, a trellis decoder is implemented based on the Viterbi algorithm. A trellis decoder utilizes the inherent memory of the CPM waveforms across multi-symbol to achieve better performance compared to a symbol-by-symbol detection. The match filter matrix is developed based on the shaping filter characteristics, which defined the phase tree of the modulation. The output of the match filter matrix is used as the branch calculator for the Viterbi algorithm [8]. The common Rx-path architecture for demodulation and detection is illustrated in Figure 8.

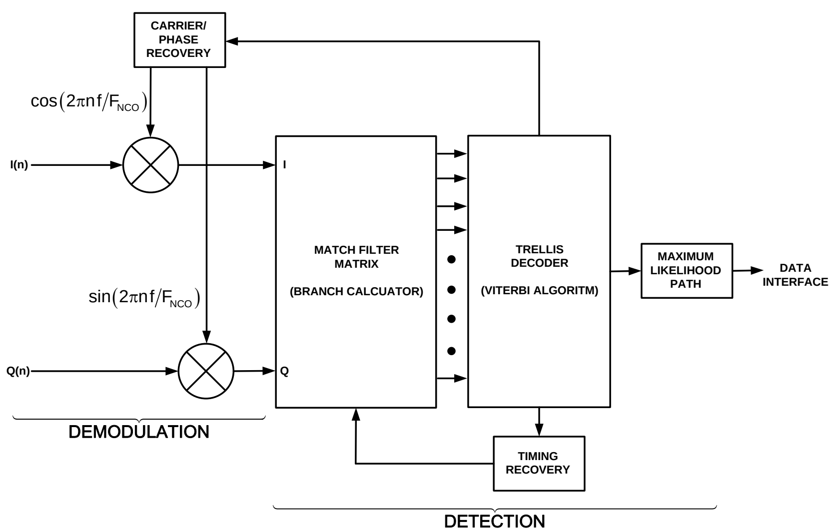

Figure 8: Rx-Path Common Hardware Architecture

CONFIGURATION AND CONTROL

The MMDR and C2 are implemented using state-of-the-art SoC technology. The SoC consists of dual-core ARM processing system (PS) integrated with a high-performance programmable logic (PL) system. In addition, dedicated hardware interfaces are available for utilization by the PS or PL. As a result, the MMDR and C2 can be implemented into a single hardware sub-system consisting of two operational planes: the digital radio plane that hosts the telemetry waveform firmware and the C2 plane that hosts the embedded software for the system configuration, control and status as illustrated in Figure 9. A FPGA mezzanine card (FMC) interface consisting of dual 12-bit 1-GSPS analog-to-digital converters and dual 16-bit 1-GHz digital-to-analog converter (DAC) is used for the high-speed data conversion.

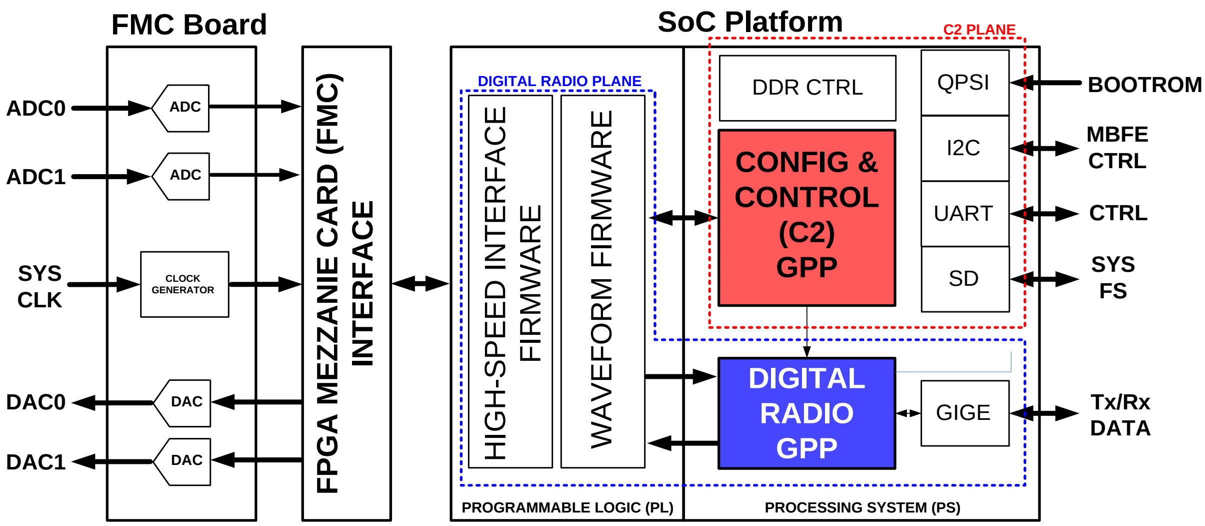

Figure 9: MMDR and C2 Hardware Sub-System

Open-source Linux is used to host the embedded software on the dual-core PS. Software components include the C2 core software and the DR general purpose processor (GPP) software. The C2 core software is responsible for general system configuration, control, and status. The DR GPP software implements the Viterbi algorithm for the detection, while the VITA Radio Transport (VRT) protocol over Gigabit Ethernet (GIGE) is implemented for the data interface. In addition to the SoC PS, a micro-controller is implemented for stand-alone configuration of the MBFE sub-system, which includes several ABPF components, automatic gain control (AGC) amplifiers, variable gain amplifier (VGA), and frequency synthesizers. Memory maps are used for control and status between the dual-core PS and PL. The hardware architecture for the C2 sub-systems is illustrated in Figure 10.

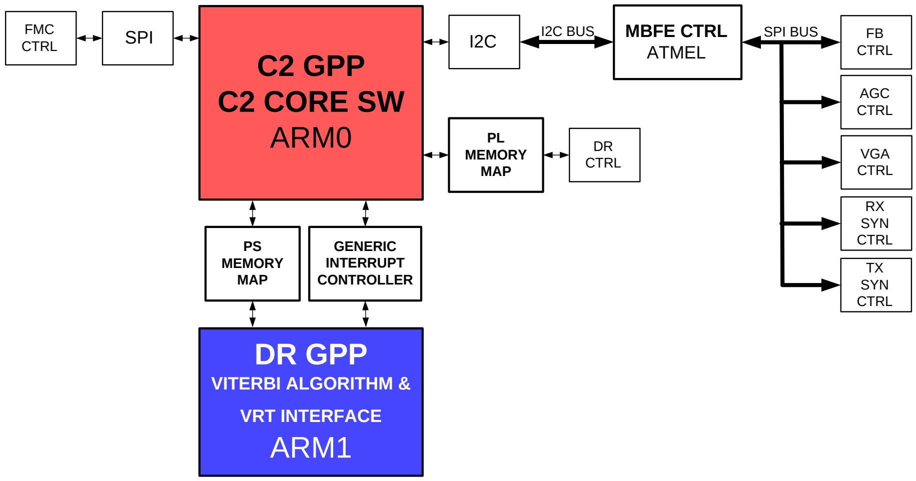

Figure 10: C2 Hardware Architecture

CONCLUSION

A system framework for a multi-band, multi-mode SDR platform was presented. The framework consists of hardware architectures for the multi-band front-end, multi-mode digital radio, and the configuration and control sub-systems. Common architectures for the transmitter and receiver channel are used to minimize development time. System-on-a-Chip (SoC) technology is used to achieve high integration between the digital radio and configuration and control sub-systems.

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